

What is claimed is:

- 1 1. An apparatus, comprising:
2 an input block to apply an input signal to a
3 common input terminal of a sensing block; and
4 a converting block to receive a sensed signal
5 from the sensing block in response to applying the input
6 signal.
- 1 2. The apparatus of claim 1, wherein the converting
2 block provides an output signal based on the sensed signal.
- 1 3. The apparatus of claim 1, wherein the converting
2 block provides a signal having a fractional pulse density
3 that is indicative of acceleration.
- 1 4. The apparatus of claim 1, wherein the input block
2 applies a first signal to the common input terminal during
3 a first clock phase and a second signal during a second
4 clock phase.
- 1 5. The apparatus of claim 1, wherein the converting
2 block integrates the sensed signal and provides a first
3 output signal and a second output signal.

1 6. The apparatus of claim 5, wherein the
2 converting block further compares the first output signal
3 and the second output signal and provides an output
4 signal.

1 7. The apparatus of claim 6, wherein the converting
2 block provides the output signal to the input block.

1 8. The apparatus of claim 1, wherein the input block
2 comprises a first input capacitor and a second input
3 capacitor, wherein the input block provides a first input
4 signal to the converting block through the first input
5 capacitor and a second input signal to the converting block
6 through the second input capacitor.

1 9. The apparatus of claim 8, wherein the input block
2 provides the first input signal through a first capacitor
3 and the second input signal through a second capacitor.

1 10. The apparatus of claim 1, further comprising a
2 storage unit to store one or more voltage values to apply
3 to the apparatus.

1 11. A method comprising:
2 providing an input signal to a common input
3 terminal of a sensing block;
4 receiving a sensed signal from the sensing
5 block based on providing the input signal; and
6 providing a signal based on the sensed signal.

1 12. The method of claim 11, comprising providing a
2 digital signal based on the sensed signal.

1 13. The method of claim 11, comprising providing
2 signal having a fractional pulse density that is
3 indicative of acceleration.

1 14. The method of claim 11, comprising providing a
2 first signal to the common input terminal during a first
3 clock phase and a second signal to the common input
4 terminal during a second clock phase.

1 15. The method of claim 14, comprising providing
2 the first signal and the second signal to the common
3 input terminal during non-overlapping clock cycles.

1 16. The method of claim 15, comprising integrating
2 the sensed signal and providing a first output signal and
3 a second output signal.

1 17. The method of claim 16, comprising comparing
2 the first output signal and the second output signal and
3 provides an output signal.

1 18. The method of claim 17, comprising providing
2 the first signal and second signal based at least in part
3 on the output signal.

1 19. An apparatus, comprising:
2 an input block to provide an input signal to a
3 common terminal of a first capacitor and a second
4 capacitor of a sensing block; and

5 a converting block to receive a sensed signal
6 from the sensing block in response to applying the input
7 signal.

1 20. The apparatus of claim 19, wherein the
2 converting block provides a digital signal based on the
3 sensed signal.

1 21. The apparatus of claim 19, wherein the input
2 block applies a first signal to the common input terminal
3 during a first clock phase and a second signal during a
4 second clock phase.

1 22. The apparatus of claim 19, wherein the input
2 block comprises a first input capacitor and a second
3 input capacitor, wherein the input block provides a first
4 input signal to the converting block through the first
5 input capacitor and a second input signal to the
6 converting block through the second input capacitor.

1 23. The apparatus of claim 19, wherein the
2 converting block comprises:

3 an integrator to receive the sensed signal from
4 the sensing block and to produce an integrated signal;

5 a comparator to receive the integrated signal
6 and to provide an output signal; and

7 a latch to receive the output signal and to
8 provide a latched output signal.

1 24. The apparatus of claim 19, further comprising a
2 storage unit to store one or more voltage values to apply
3 to the sensing circuit.

1 25. A restraint system, comprising:
2 a sensing circuit to:
3 apply an input signal to a common input
4 terminal of a sensing block;
5 receive a sensed signal from the sensing
6 block in response to applying the input signal; and
7 provide an output signal based at least in
8 part on the sensed signal; and
9 a deployment block to provide an activation
10 signal based at least in part on the output signal from
11 the sensing circuit.

1 26. The restraint system of claim 25, wherein the
2 deployment block provides the activation signal to
3 activate an airbag.

1 27. The restraint system of claim 25, wherein the
2 sensing circuit is clocked using a plurality of non-
3 overlapping clocks.

1 28. The restraint system of claim 25, wherein the
2 sensing circuit provides a digital signal.

1 29. The restraint system of claim 25, wherein the
2 sensing circuit provides a signal having a fractional
3 pulse density that is indicative of acceleration.

1 30. The restraint system of claim 25, further
2 comprising a storage unit to store one or more voltage
3 values to apply to the sensing circuit.